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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 09/998,848	**Applicant(s)** OGAMI, KENNETH Y.	
	Examiner Ted T. Vo	**Art Unit** 2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14, 16-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed on 05/07/2007.

Claims 1-14, 16-35 are pending in this application.

Response to Arguments

2. Applicants' arguments in the Remarks section filed on 05/07/2007 have been respectfully considered.

The reference shows exactly the tool disclosed by the application used for claiming. See the Figure in the reference last page (page 11), and Application's Figures 6-7. It should be noted that Bindra is a barred reference. In the Applicants' remarks, the argument appeared that the tool of Bindra cannot not do their claims. Examiner disagrees.

Furthermore, Examiner only stated in the prior actions: "Bindra does **not explicitly** address **the claimed statement**, "*automatically constructing source code*". However, the tool itself under the 103 obviously does exactly what the Applicants' claiming, "*automatically constructing source code*". If the tool shown in the Bindra does not do the functionality as recited in the claim, then this tool cannot work and meaningless, then each of virtual blocks shown in the tool is functionless. It should be noted that the Applicants' claim is to include only "automatically construct", where the Bindra shows executable module and it is already there to connect with each of virtual blocks, where configuration data is already there (as shown in the Figure 4, and the same shown in the Application's specification) for connecting with the module. The act of "automatically" is clearly done by the tool of figure 4. Therefore, it does not need a Bindra's statement, "Automatically Construct", until this application brings out preemption; the tool shown in the Figure 4 performs this. All ordinary in the art would recognize "automatically construct" because of inherency or enablement. Applicants require the office for a second reference to say "automatically construct", it is improper, where the term "automatically construct" does not present a patentable element, but only a preemption of the function done by the tool shown in the prior art, and also admitted by Applicants (via their affidavits filed on 08/18/2005).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-14, 16-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bindra, "Programmable SoC Delivers A New Level Of System Flexibility", 2000.

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per Claim 26: Bindra discloses a PSoC Designer that is used to configure and construct code for a microcontroller; the disclosure covers the limitations,

A computer system comprising a processor coupled to a bus, a display device coupled to said bus, and a memory coupled to said bus, said memory containing instructions to implement a method for configuring a microcontroller, said method comprising:

displaying a collection of virtual blocks in a design system with each virtual block in said collection corresponding to a programmable block in said microcontroller (Bindra: P.11, Figure 4, the system in the Figure 4 displays a collection of virtual blocks);

receiving a selection of a user module defining a function (Bindra: Figure 4: "User Modules Selected for Placement": E.g. the system of Figure 4 receives the selection of a user from selecting circuit block icons in the right top section. The selection of circuit block icons is implemented in a combination shown within the right bottom section);

assigning a virtual block taken from said collection to said user module (Figure 4, Each block in the circuit in the right bottom section in Figure 4 could be assigned in this section from selection of "User Modules" in the right top section; configuration information and connection are assigned by dialog section in the left section and the buttons given in the top rows of the PSoC Designer Tool); and

For the limitation, ***automatically constructing*** *assembly code holding configuration information for a programmable block corresponding to said virtual block to perform said function*", Bindra discloses Figure 4 and its below illustration "device editor employs a graphical interface to connect **user modules**, which are next mapped onto the SoCblocks on-chip.

The user module = *assembly code holding configuration information*. For '*configuration information*', refer to "Global Resources" and "Placement parameters" in the left section of Figure 4.

i.e., Bindra does not explicitly address the claimed statement, "*automatically constructing source code".*

However, *automatically constructing* is an enablement of a virtual block which is known in the art as the programming code or the code in the user module representing the circuitry function of the virtual block so that when a circuit is built/simulated, **the PSoc will automatically connect the code internally to the virtual block** so that the code yield the same and predictable results to the function indicated as name of the virtual block. For example, a virtual block is a digital converter ADC then the assembly code has the configuration information corresponding to the configuring data shown in the right of the Figure 4.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to know that, for an enablement, every user module in the PSoC Designer discussed by Bindra is "code" that **is automatically connected** to a corresponding virtual block when a circuit is built in the system, PSoc Designer, shown by Bindra.

(Note, the Tutorial Revision 1.0, "PSoC Designer: Integrated Development Environment", 7-2001 admitted that any circuitry of virtual blocks built in the PSoC Designer, the code representing to each virtual block is automatically connected – i.e. for enablement, the virtual blocks, shown as statutory barred diagram by Bindra, must be automatically constructed with assembly code so that the circuits result functionality. This is similarly as an admitted prior art).

As per Claim 27: Regarding limitation, "The computer system of Claim 26, wherein said collection is displayed as a two dimensional array", see collection in the right bottom section of Figure 4.

As per Claim 28: Regarding limitation, *The computer system of Claim 26, wherein said assigning further comprises assigning a second virtual block to said user module*, it is either one of other blocks shown the right bottom section of Figure 4.

As per Claim 29: Regarding limitation, *The computer system of Claim 26, wherein said assembly code further comprises a symbolic name for a register address in said programmable block*, it is the code generated by the PSoC Design to the collection shown in the right bottom section of Figure 4, where the symbolic name for a register address is done by register mapping as addressed above.

As per Claim 30: Regarding limitation, *The computer system of claim 26 wherein said symbolic name is derived from said function*, it is functionalized to a circuit element, and based on pins assignment to the user module.

As per Claim 1:

Bindra discloses a PSoC Designer that is used to configure and construct code for a microcontroller; the disclosure covers the limitations,

A method for configuring a microcontroller, comprising:

displaying a collection of virtual blocks in a design system with each virtual block in said collection corresponding to a programmable block in said microcontroller (Bindra: See P.11, Figure 4);

receiving a selection of a user module defining a function (Bindra: See Figure 4: "User Modules Selected for Placement": E.g. see circuit block icons in the right top section which will be implemented in a combination shown within the right bottom section in the Figure 4);

assigning a virtual block taken from said collection to said user module (See Figure 4, Each block in the circuit in the right bottom section in Figure 4 could be assigned in this section from selection of "User Modules" in the right top section; configuration information and connection are assigned by dialog section in the left section and the buttons given in the top rows of the PSoC Designer Tool);

For the limitation, *automatically constructing source code comprising configuration information for a programmable block of said microcontroller corresponding to said virtual block wherein said configuration information is used to cause said programmable block to implement said function*, Bindra suggests (Figure 4 and its below illustration) "which are next mapped '*automatically constructing*' onto the SoCblocks on-chip '*assembly code holding configuration information*'. For '*configuration information*', refer to "Global Resources" and "Placement parameters" in the left section of Figure 4,

i.e., Bindra does not explicitly address the claimed statement, "*automatically constructing source code*".

However, *automatically constructing* is an enablement of a virtual block which is known in the art as the programming code or the code in the user module representing the circuitry function of the virtual block so that when a circuit is built/simulated, the PSoc will automatically connect the code to the virtual block.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to know that, for an enablement, every user module in the PSoC Designer discussed by Bindra is "code" that is automatically connected to a corresponding virtual block when a circuit is built in the system, PSoc Designer, shown by Bindra.

As per Claim 2: Bindra further discloses,

The method of Claim 1, wherein said function comprises a pulse width modulator (Bindra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 36, "PWMs").

As per Claim 3: Bindra further discloses, *The method of Claim 1, wherein said function comprises a timer.* (Bindra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 36, "*timers*").

As per Claim 4: Bindra further discloses, *The method of Claim 1, wherein said function comprises an analog-to-digital converter* (Bindra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 35, "ADCs").

As per Claim 5: Bindra further discloses, *The method of Claim 1, wherein said function comprises a digital-to-analog converter* (Bindra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 35 "DACs").

As per Claim 6: Bindra further discloses, *The method of Claim 1, wherein said function comprises a counter* (Bindra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 36 "counters").

As per Claim 7: Bindra further discloses, *The method of Claim 1, wherein said function comprises a signal amplifier.* (See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 33 *"differential amplifiers"*).

As per Claim 8: Bindra further discloses, *The method of Claim 1, wherein said function provides serial communication.* (See Figure 4, refer to "User Module" that represents various Digital functions, and see P.3, line 9, "serial transmitters/receivers").

As per Claim 9: Bindra further discloses, *The method of Claim 1, wherein said collection is displayed as a two dimensional array of programmable analog virtual blocks and programmable digital virtual blocks.* (See collections in the right bottom section, which is *two-dimensional array*).

As per Claim 10: Bindra further discloses, *The method of Claim 1, wherein said assigning further comprises assigning a second virtual block to said user module* (See collections in the right bottom section, which is two *dimensional array*).

As per Claim 11: Bindra further discloses, *The method of Claim 1, wherein said source code comprises a symbolic name for a register address in said programmable block.* (Bindra: See page 2, lines 12-17 ('register space that holds the configuration information').

As per Claim 12: Bindra further discloses, *The method of Claim 11 wherein said symbolic name is derived from said function.* (See Bindra 'User module" in Figure 4, where user module represents a circuit element. Each circuit element is a symbolic name function: e.g.: ADC, DAC, Timer, Counter, etc).

As per Claim 13: Bindra disclosure covers the limitations,

A method of configuring a microcontroller having a programmable block, said method comprising:

receiving a selection of a user module defining a circuit design (Bindra: See Figure 4: "User Modules Selected for Placement": E.g. see circuit block icons in the right top section which will be implemented in a combination shown within the right bottom section in the Figure 4);

assigning a virtual block in a design system where said virtual block corresponds to said programmable block (See Figure 4, Each block in the circuit in the right bottom section in Figure 4 could be assigned in this section from selection of "User Modules" in the right top section; configuration information and connection are assigned by dialog section in the left section and the buttons given in the top rows of the PSoC Designer Tool); *and*

For the limitation, *automatically constructing assembly code comprising configuration information for said programmable block to implement said circuit design, wherein said assembly code is constructed from template assembly code by substituting information specific to said user module and information specific to said circuit design for generic information in said template assembly code,* Bindra suggests (Figure 4 and its below illustration) "which are next mapped '*automatically constructing*' onto the SoCblocks on-chip '*assembly code holding configuration information*'. For '*configuration information*', refer to "Global Resources" and "Placement parameters" in the left section of Figure 4,

i.e., Bindra does not explicitly address the claimed statement, "*automatically constructing source code".*

However, *automatically constructing* is an enablement of a virtual block which is known in the art as the programming code or the code in the user module representing the circuitry function of the virtual block so that when a circuit is built/simulated, the PSoc will automatically connect the code to the virtual block.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to know that, for an enablement, every user module in the PSoC Designer discussed by Bindra is "code" that is automatically connected to a corresponding virtual block when a circuit is built in the system, PSoc Designer, shown by Bindra.

As per Claim 14: Regarding,

"The method of Claim 13, wherein said automatically constructing further comprises:

computing a register address for a register within said programmable block; determining a symbolic name for said register address, said symbolic name corresponding to said user module and said circuit design; and substituting said symbolic name for a generic name in said template assembly code". See page 2, lines 12-17 ('register space that holds the configuration information') and page 6, lines 7- 13, ('user modules are selected, pins are assigned, and register mapping are establish');

- *computing a register address for a register within said programmable block:* page 6, lines 7- 13, referring "register mapping"
- *determining a symbolic name for said register address, said symbolic name corresponding to said user module and said circuit design:* page 2, lines 12-17, referring "holds the configuration information".
- *substituting said symbolic name for a generic name in said template assembly code:* referring the code construction performed by the PSoC Designer.

As per Claim 16: regarding limitations of Claim 16.

See page 2, lines 12-17 ('register space that holds the configuration information') and page 6, lines 7- 13, ('user modules are selected, pins are assigned, and register mapping are establish') for

- *determining a symbolic name corresponding to said user module and said circuit design;* referring "holds the configuration information".
- *computing a register address for a register within said programmable block;* referring "register mapping"
- *assigning said symbolic name to said register address; and placing said symbolic name into said assembly code in place of a generic name provided in said template assembly code file:* referring the code construction performed by the PSoC Designer.

As per Claim 17: See rationale addressed in the rejection of Claim 13 above.

As per Claim 18: See rationale addressed in the rejection of Claim 14 above.

As per Claim 19: See rationale addressed in the rejection of Claim 14 above.

As per Claim 20: See rationale addressed in the rejection of Claim 16 above.

As per Claim 21: See rationale addressed in the rejection of Claim 13 above.

As per Claim 22: See rationale addressed in the rejection of Claim 14 above.

As per Claim 23: See rationale addressed in the rejection of Claim 14 above.

As per Claim 24: See rationale addressed in the rejection of Claim 16 above.

As per Claim 25: See rationale addressed in the rejection of Claim 13 above.

As per Claim 31: Bindra disclosure covers the limitation:

A computer implemented method of generating program information for a programmable electronic device, said method comprising:

a) accessing a selected a user module, wherein said user module is defined by a first data structure; (Bindra: See Figure 4: "User Modules Selected for Placement"- E.g. see circuit block icons in the right top section implemented in a combination shown within the right bottom section in the Figure 4);

b) placing said user module within a second data structure that defines a hardware resource of said programmable electronic device; (See Figure 4, Each block in the circuit in the right bottom section in Figure 4, could be assigned in this section from selection of " User Modules" in the right top section; configuration information and connection are assigned by dialog texts in the left section buttons on the top of the PSoC Designer Tool. When running the Tool, each user module assigned in the collection in the right bottom section will be assigned accordingly);

"c) using said first and second data structures to automatically generate first source code for realizing said user module within said hardware resource; and

d) saving said first source code in a computer file"

(Bindra: For this limitation, see Figure 4 and its below illustration: "which are next mapped onto the SoCblocks on-chip", '*using said first and second data structures*'. For *saving said first source code in a computer file*: refer to 'File", 'Edit', 'View' on the top of the PSoC Designer Tool).

For the limitation in c) "*automatically generate first source code for realizing said user module within said hardware resource",* Bindra suggests (Figure 4 and its below illustration) "which are next mapped '*automatically generate*' onto the SoCblocks on-chip '*realizing said user module within said hardware resource*',

i.e., Bindra does not explicitly address the claimed statement, "*automatically generate first source code".*

However, *automatically generate* is an enablement of a virtual block which is known in the art as the programming code or the code in the user module representing the circuitry function of the virtual block so that when a circuit is built/simulated, the PSoc will automatically connect the code to the virtual block.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to know that, for an enablement, every user module in the PSoC Designer discussed by Bindra is "code" that is automatically connected to a corresponding virtual block when a circuit is built in the system, PSoc Designer, shown by Bindra.

As per Claim 32: regarding limitation,

A method as described in Claim 31 further comprising:

e) accessing parameter values that define the behavior of said user module such that it operates in a prescribed manner, (Bindra: See left section in Figure 4);

f) automatically generating second source code, based on said parameter values, for causing said user module of said hardware resource to behave in said prescribed manner (Bindra suggests (Figure 4 and its below illustration) "which are next mapped '*automatically generating*' onto the SoCblocks on-chip '*hardware resource to behave in said prescribed manner*'; *and*

g) saving said second source code in a computer file (Bindra: See Figure 4, icons in the top rows used to save a file).

As per Claim 33: Bindra further discloses, "*A method as described in Claim 32 further comprising using said first and second source code to program said programmable electronic device*" because it the collection in Figure 4 would be mapped to a real design.

As per Claim 34: Bindra further discloses, *A method as described in Claim 33 wherein said programmable electronic device is a microcontroller*. See Bindra's Figure 1.

As per Claim 35: Bindra further discloses, *A method as described in Claim 31 wherein said a) and said e) are performed using a graphical user interface,* because PSoC Designer is a GUI.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708.

The facsimile number for the organization where this application or proceeding is assigned is the Central Facsimile number **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TTV
August 03, 2007

TED VO
PRIMARY EXAMINER